

## REMARKS

Claims 1 and 6 have been amended. Claims 1 to 25 remain active in this application and claims 26 to 32 which were non-elected have been canceled.

Claims 1 to 25 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The rejection is respectfully traversed.

Claim 1, for example, is readable on Fig. 2 as follows:

A semiconductor device comprising:

- a semiconductor chip (201) having a planar active surface (201a) including an integrated circuit, said integrated circuit having metallization patterns including a plurality of contact pads at said planar active surface (202);

- a protective overcoat over said planar active surface, said protective overcoat including windows exposing said plurality of contact pads, said windows having sidewalls (203 and/or 204);

- an added conductive layer covering each of said contact pads, said window sidewalls, and a portion of said protective overcoat surrounding said windows, said added layer having a surface conforming to said contact pads, said window sidewalls, and said portion of said protective overcoat adjacent said chip and a planar outer surface (206 with or without 205 and with or without 207)

As can be seen, the conductive layer 206 has a planar surface and the other surfaces of this layer are conformal to the contact pad 206 and the sidewalls of the window formed by the layers 203 and 204 and it extends over the planar outer surface. The "window" is the cut out region shown in layers 203 and 204 which is a window through these layers to the contact pad. The above argument applies as well to the other independent claims.

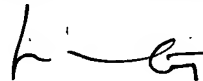
Claims 1 to 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art as shown in prior art Fig. 1 of the subject application. The rejection is respectfully traversed.

All of the claims require that the added conductive layer covering each of the contact pads, the window sidewalls, and a portion of the protective overcoat

surrounding the windows, the added layer having a surface conforming to the contact pads, the window sidewalls, and the portion of the protective overcoat adjacent the chip and a planar outer surface. This layer in Fig. 1 does not have a planar outer surface but rather is also conformal to the layers between that layer and the layers intervening to the chip. As stated in the paragraph bridging pages 12 and 13 of the specification, this layer has the important function to enable the transition from a conformal outline following the chip surface contours, to a "flat" outline defining a planar outer surface, which is substantially parallel to the chip surface. Advantages of this type of structure are set forth in the specification in the SUMMARY OF THE INVENTION from page 4, line 7 to page 5, line 17.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



Jay M. Cantor  
Attorney for Applicant(s)  
Reg. No. 19,906

Texas Instruments Incorporated  
P. O. Box 655474, MS 3999  
Dallas, Texas 75265  
(301) 424-0355 (Phone)  
(972) 917-5293 (Phone)  
(301) 279-0038 (Fax)